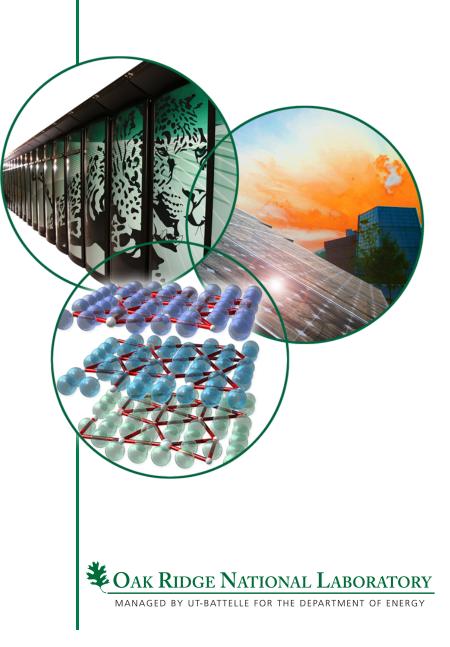
RRD Software Engineering

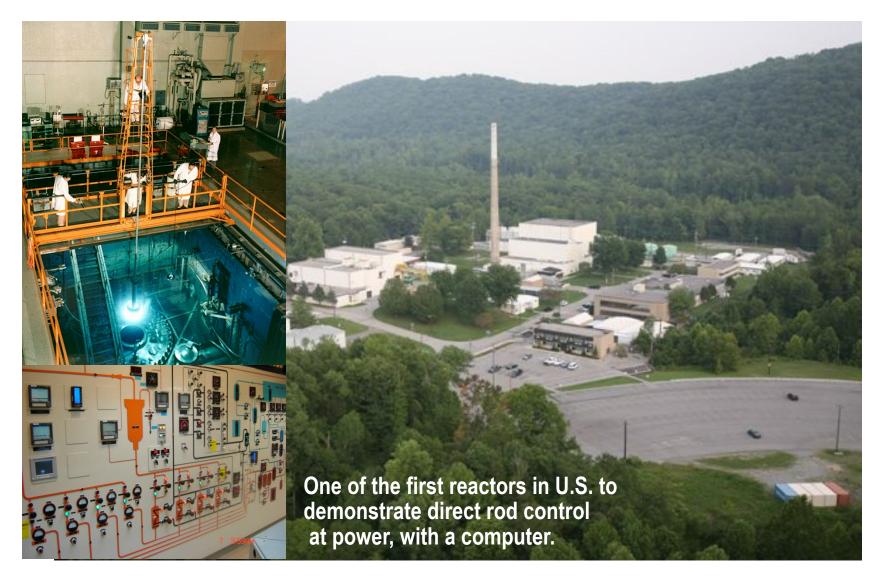
Digital Systems at the HFIR

September 20, 2010





High Flux Isotope Reactor

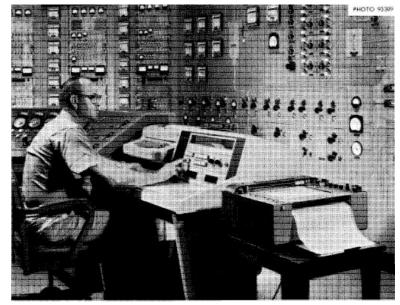




HFIR On-Line Computer



- 32K Memory
- Fortran Language
- Teletypewriter
- \$275,000



CDC-1700 Computer by Control Data Corporation



Plant Computer



PDP-11/60 by Digital Equipment Corporation



Balance of Plant Computer



Intel 80486 CPU by Northgate



Digital Instruments

Transmitters by Yokogawa







Recorder by Chessell



Programmable Logic Controllers (PLC)





Programmable Logic Controllers





Software Quality Assurance

Conformance to:

- explicit functional and performance requirements,
- explicitly documented development standards, and
- implicit characteristics

that are expected of all professionally developed software.



Software Engineering

The application of a systematic, disciplined, and quantifiable approach to software development, operation, and maintenance.

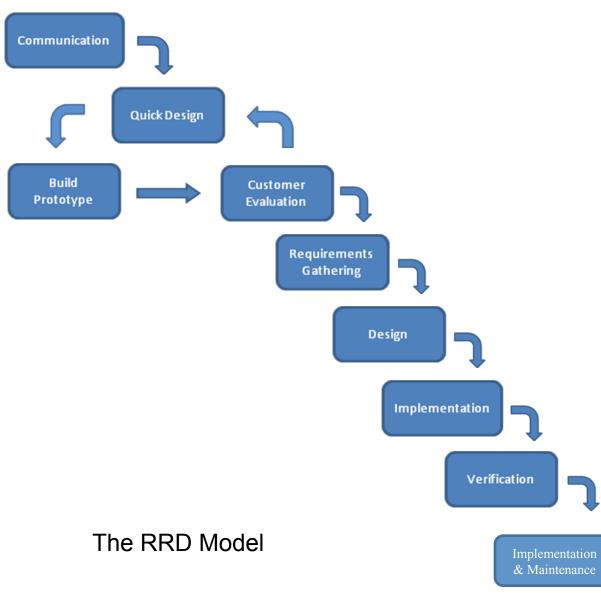


Process Development Input



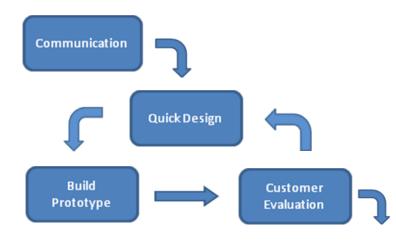


Process Models





Prototype Phase



- •Begin Team Meetings
- •Discuss Functionality and General Design
- •Purchase Hardware for Evaluation
- •Setup Network
- •General HMI
- •Training



Detailed Design Phase



Write Functional Description and SQA Plan
Requirements Walkthrough
Review of FD and SQAP



Write SRS and SQA Umbrella Documents
Review of SRS and SQA
Process Audit by QA





Implementation Phase



Implementation & Maintenance

•Write Code

Code Walkthrough

•Review of Code

•Write SRL and Test Plans

•Review of SRL and Test Plans

•Perform Testing

•Final Audit by QA

•Write Backup/Recovery Plans

•Write Maintenance Plan

•Review of Plans

•Work Closeout



Metrics

Classifications

Logic Problem																						
	Forgotten cases or steps				A100																	
	Duplicate logic			A200																		
	Extreme conditions neglected			A300																		
	Unnecessary function			A400																		
	Misinterpretation				A500																	
	Missing condition test			1	A600																	
	Checking wrong variable				A700																	
	Iterating loop incorrectly			i i	A800																	
Computation Problem				- (
	Equation insufficient or incorrect			B100																		
				B110																		
	Operand in equation incorrect			B120																		
	Operator in equation incorrect			B130																		
	Parenthesis used incorr	Parenthesis used incorrectly			B140																	
	Precision Loss			B200																		
	Rounding or truncatio	[C.A.	wara D	orrolon		Vetrica	C								
	Mixed modes	System: System: Date: Deployment: Pre or Post								-												
	Sign convention fault	Deployment Age:																				
Interface/Timing Problem		Source	Class	Qty	Class	Qty	Class	Qty	Class	Qty	Class	Qty	Class	Qty	Class	Qty	Class 🤇	ty C1	ass	Qty	Class	Qty
	Interrupts handled incorre	Al	A 100		A200		A300		B100		B110		B120		B130		B200	c	.00		C200	
	I/O timing incorrect	A2	D100 A100		D200 A200		D210 A300	-	D220 B100		D230 B110		E100 B120		E200 B130	6 8	E300 B200		00		F200 C200	
	Timing fault causes da		D100	1	D200	ĺ.	D210		D220		D230		E100		E200		E300	F	.00		F200	
	Subroutine/Module mism	A3	A100 D100		A200 D200		A300 D210		B100 D220		B110 D230		B120 E100		B130 E200		B200 E300	F	.00 00		C200 F200	
	Wrong subroutine call	A4	A100 D100)	A200 D200		A300 D210		B100 D220		B110 D230		B120 E100		B130 E200		B200 E300	C. F	.00 00		C200 F200	
	Incorrectly located sul	B1	A 100 D 100		A200 D200		A300 D210		B100 D220		B110 D230		B120 E100		B130 E200		B200 E300		.00 00		C200 F200	
	Nonexistent subroutin	B2	A100 D100)	A200 D200	<u>)</u>	A300 D210		B100 D220		B110 D230		B120 E100		B130 E200		B200 E300	C.	00		C200 F200	0 1
	Inconsistent subroutin	B3	A100	2	A200	2	A300	()	B100		B110		B120		B130	(<u> </u>	B200	C	.00		C200	1
Data Handling Problem		Cl	D100 A100		D200 A200	8	D210 A300		D220 B100		D230 B110		E100 B120		E200 B130		E300 B200	C	00		F200 C200	
	Initialized data incorrectly	C2	D100 A100		D200 A200	/	D210 A300		D220 B100		D230 B110		E100 B120		E200 B130		E300 B200		00		F200 C200	
	Accessed or stored data i	C3	D100 A100		D200 A200	1	D210 A300		D220 B100		D230 B110		E100 B120		E200 B130		E300 B200	F	00		F200 C200	
	Flag or index set incor		D100		D200		D210		D220		D230		E100		E200		E300	F	00		F200	
	Packed/unpacked data	Dl	A100 D100		A200 D200		A300 D210		B100 D220		B110 D230		B120 E100		B130 E200		B200 E300	F	.00 00		C200 F200	
		D2	A100		A200	8	A300		B100		B110	S - 3	B120		B130	S	B200		.00		C200	8 - 8
	Referenced wrong dat		D100		D200		D210		D220		D230		E100		E200		E300	ा	00		F200	



Metrics Example

Defect Tracking Sheet

Date	Origin	Description	Severity	Classification	Resolution
02/18/2010	Requirements	Annunciator Text Missing	4	F400	Fix at next revision. Review HMI structured walk through requirements.

Origin:

Requirements (missing from FD) Design (prototype doesn't work) Code (wrong instruction in code) Testing (test plan incomplete) Secondary (bad fixes/changes)

Severity:

- 1 Unanticipated SCRAM
- 2 Operator Action
- 3 Operator Work Around
- 4 Cosmetic



Digital Upgrades





Control Rod Time-Of-Flight PLC



Cold Source Distributed Control System

Digital Upgrades



HFIR Data System

Wide Range Counting Channel



Summary

- Digital Controls are not new to HFIR
- Online Computer successful at calculating reactivity and performing rod control
- Successful Software Development Process
- Process Validation = History + Metrics
- Digital Upgrades are the future.

